Power Minimization Techniques

Data centers are facing unprecedented challenges to reduce space, cooling, power and cost. These pressures are creating a focus on providing equipment with highly optimized power characteristics. This focus minimizes both the cost of electricity and cooling in data centers, carrier facilities as well as high-performance enterprises.

This white paper provides a high-level overview of certain design techniques Force10 Networks incorporates into the ExaScale E-Series core switch/router in order to minimize power consumption.

Introduction

Network operators, such as data centers, high-performance enterprises and service providers, are increasingly making power efficiency a critical part of their communications equipment buying criteria. According to IDC, the monthly power and cooling costs for a data center can be as much as 25% of the overall operations budget. Enterprises and service providers have similar concerns for their own network facilities. As one measure, many large data center operators (ex: large portals like Google and MSN) build out their facilities in locations that provide access to power and cooling resources at the lowest cost. Beyond this, a national focus on green technology is driving purchasing decisions and subsidies.

Equipment developers have many techniques for minimizing power in communications equipment at their disposal. In order to fully leverage these techniques, they must be incorporated as a design objective from the outset of the development cycle. This white paper describes a number of high level techniques that Force10 Networks has incorporated into the design of the ExaScale E-Series® core switch/router line in order to provide industry leading (low) power consumption. A number of these techniques are generally available to the industry; however, some of the techniques are covered by our intellectual property and not generally available.

At a very high level, the areas of development focus for the ExaScale E-Series are as follows:

- Power system design
- ASIC design
- Functional integration and compaction
- Density

Power System Design

The power and distribution subsystems in the E-Series architecture have been specifically designed to provide high efficiency with very low loss across a multitude of temperature ranges. By utilizing high quality switching supplies optimized for low voltage and high current, the E-Series architecture is inherently more efficient. In addition to the switching supplies, the overall power efficiency is predicated upon the design of the power distribution subsystem, which is comprised of the components between the power supplies and the loads, such as the connectors, backplanes, modules, cabling and decoupling.
In earlier generation designs, the primary contribution to loss in DC (direct current) distribution systems was based upon resistive losses. However, with increased power consumption resulting from the use of high performance Ethernet NPUs (Network Processor Units) with Traffic Manager functionality, capacitive reactive power loss is now an equal threat to the power distribution system. As such, minimizing both types of losses between the power supply and the load(s) is now a design goal. This reduces the amount of power dissipation wasted by the distribution system and incremental contribution loss in the power supply.

Chassis-based systems do limit the physical placement options of the power supplies and the load(s). As such, minimizing the losses in the power distribution subsystem is the primary optimization path. Force10 Networks has a number of patents covering techniques for implementing low-loss power distribution in a backplane environment. These techniques are incorporated in the E-Series platform.

**ASIC Design**

The ExaScale line cards and SFMs (switch fabric modules) for the E-Series product are implemented with a number of custom ASICs (Application Specific Integrated Circuits) developed by Force10 Networks. This facilitates a minimal number of devices on the I/O cards while providing a high degree of functionality with a low power focus.

There are a number of techniques that have been used to minimize the power consumption of the system based upon the ASIC architecture.

**Functional integration** – Integrating high levels of functionality minimizes the number of physical devices in the system and saves overall power. The level of the integration designed into the ExaScale ASICs is extremely high. Ethernet MACs are integrated into the ASICs as are the backplane serialization / deserialization (SERDES) components. By way of example, the ExaScale ASICs include in excess of 60 million gates. By utilizing fewer chips than competitive products, the ExaScale delivers lower overall power consumption.

**Libraries** – ASIC libraries typically include both high power (highest performance) and low power instances of logic functions. Low power functions are preferentially used in the ASICs.

**Logic structure** – During compilation (translation from register transfer level to gates) there is the option to build either lower or higher power structures. Higher power structures tend to be more prolific of gates (usually flattened) as opposed to more hierarchical structures.

**Floor planning** – Power dissipation in an ASIC is often a function of the amount of capacitance that a gate must drive. This can be minimized due to careful floor planning.

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**Figure 2. Force10 ASIC Chipset — ExaScale**

- Single chip for 50 Gbps Ingress or Egress
- Line-rate IP, Layer 2, MPLS and ACLs
- Flexible Packet Classification
- Line-rate External Memory Traffic Manager with 8 Queue Support
- 3.5 Tbps Switch Fabric Capacity
**Functional Integration and Compaction**

The ExaScale technology has been designed around sharing resources to minimize overall power consumption. In contrast, competitive systems tend to use resources on a dedicated basis and therefore use more of them.

In particular, CAMs (content addressable memories) and SRAMs tend to be very power consumptive. The ExaScale technology has been designed to minimize the number of CAMs and SRAMs by compacting databases and incorporating multiple lookup tables into a single physical memory array.

CAMs are used for lookup functions associated with forwarding decisions. They include Layer-2/Layer-3 lookups and ACL (access control list) lookups. The functions that use CAMs are:

- Layer-2/Layer-3 Lookup CAM
- Ingress Layer-2/Layer-3 ACL CAM
- Egress Layer-2/Layer-3 ACL CAM

The ExaScale E-Series implements all the above functions using single CAM system. The shared use of the CAM requires additional software that intelligently manages the CAMs; however, there is a significant overall reduction in system power consumption by doing so. ExaScale technology further utilizes very compact data structures and an efficient database implementation (variable length database) that minimizes the amount of SRAM required in the system and reduces power consumption. Finally, the ExaScale line cards do not use daughter cards as they also increase the amount of power dissipation in the system. Daughter cards require drivers to enable the mother board and daughter board to communicate. The drivers are consumptive of power and eliminating the need for them also lowers overall power consumption.

**Density and Non-Blocking Performance**

Port density is a primary consideration in minimizing power in any network design. We believe the ExaScale E-Series core switch/router offers the highest port density per rack inch in the industry. With high port density, networks can process more IP traffic per card, leaving more chassis space available for increased bandwidth demand. This enables customers to deploy more compact, high performance and scalable networks cost effectively. Additionally, our solutions provide industry leading bandwidth per rack inch. The distributed hardware architecture and modular operating system of the ExaScale E-Series was specifically designed to deliver non blocking, line-rate throughput and enable the network to perform at the aggregate capacity of each port.

The routing/switching requirements are based upon bandwidth needs and that cause customers to deploy capacity. The Force10 switching solutions, including the ExaScale E-Series, are designed to enable maximum network capacity utilization by minimizing performance bottlenecks even under heavy traffic conditions. These non-blocking, line-rate solutions minimize congestion and meet latency requirements for real-time application delivery.
The industry leading, non-blocking line rate port density of the ExaScale E-Series core switch/router equates to very low power contribution per port. In addition, high density means that the fixed system power consumption is amortized over greater system capacity (ports) and there is a lower power penalty based upon the fixed dissipation of the system.

**Summary**

Low power dissipation (and low cost, high density) has been design goals throughout the development of the ExaScale E-Series core switch/router. Force10 Networks has developed a number of techniques (covered by intellectual property) to minimize power dissipation. As a result, ExaScale has much lower power dissipation than competitive products, translating to much lower operational costs for carriers and data center providers.